Amendments to the Specification

Please replace the paragraph beginning at page 1, line 23 with the following amended paragraph:

Passive floating FET mixers are known in the art. A floating FET configuration uses an electrically symmetrical FET, whose drain and source terminals float with respect to ground and are coupled to the output port via a balun, as described in Vasile, C. F., Floating GASFET Circuits Offering Unique Signal Processing from DC-EHF, 1985 GOMAC Proceedings, Pp.305-309, 1985, incorporated herein by reference in it's entirety. Fig.1, taken from Vasile's article, shows a single floating FET **101** configuration. An alternative floating FET configuration which replaces the single transistor with two transistors **201** and **202** in series is shown in Fig. 2, also taken from Vasile's article. U.S. patent 4,705,967, issued for an invention of Vasile and incorporated herein by reference in it's entirety, discloses a floating multifunction FET circuit that may be used as a mixer, as shown in Fig. 3. The IF is extracted from the same side of the balun **328** as the RF signal. Therefore, the balun **328** in this design must be large to account for both the higher frequency RF signal and the lower frequency IF signal. Additionally, the RF and IF signals are not isolated, resulting in possible distortion of these signals.

Please replace the paragraph beginning at page 1, line 23 with the following amended paragraph:

Mourant, in US. patent 5,697,092 and in "A Low cost Mixer for Wireless Applications," 1995 IEEE Microwave Systems Conference pp. 21-24, also discloses similar subject matter pertaining to passive floating FET mixers, each of which is hereby incorporated herein by reference in its entirety. In U.S. patent 5,697,092, a single, floating FET mixer suitable for compact construction is disclosed, as shown in Fig. ~~42~~, taken from Mourant. The balanced IF created in the FET mixer is extracted at the RF

balun **403** in an unbalanced manner, being diplexed from the balun center tap. A series inductor **414** and capacitor **415** resonates at the RF frequency and shorts out center tap **412** to ground **406**. At low frequencies, the capacitor **415** is an open, allowing the IF **416** to be extracted. The balun **403** is fabricated with primary and secondary windings consisting of planar metal spirals that are interleaved with one another, as described by Mourant, col. 4, lines 11-18. One problem with this design is that adding a centertap to a balun adds steps to the manufacturing process. Additionally, the centertap position must be located, requiring calculation and testing. Another problem is that the IF output leads must cross over portions of the interleaved windings, making it susceptible to parasitic capacitance.